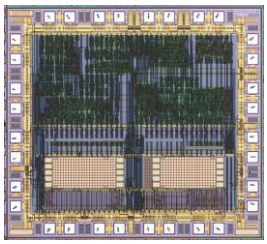
Capacitive 8-channel proximity switch with auto-calibration and very low power consumption



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1 General Description

The integrated circuit MS8885B is a capacitive 8-channel proximity switch that uses a patented (EDISEN) method to detect a change in capacitance on remote sensing plates.

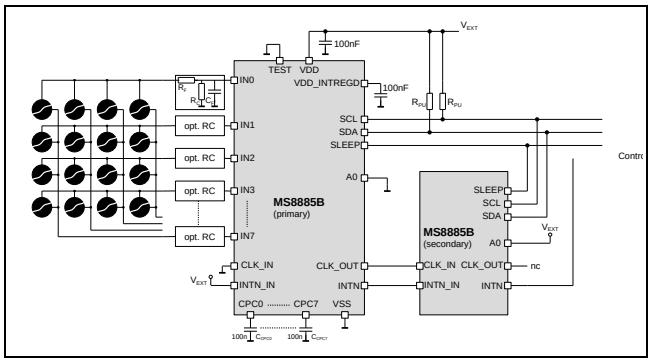
Changes in the static capacitances (as opposed to dynamic capacitance changes) are automatically compensated using continuous auto-calibration. Remote sensing plates (e.g. conductive foil) can be connected to the IC using coaxial cable.

The eight input channels operate independently of each other. There is also a built in option for a matrix arrangement of the sensors (interrupt generation only when two channels are activated simultaneously, suppression of additional channel outputs when two channels are already active).

2 Applications

- Hermetically sealed keys on a keyboard
- Switch for medical applications
- Switch for use in explosive environments
- Vandal proof switches
- Automotive: Switches in or under the upholstery, leather, handles, mats and glass
- Portable communication & entertainment units
- White goods
- Buildings: Switch in or under carpets, glass or tiles
- Sanitary applications: Use of standard metal sanitary parts (e.g. tap) as switch

3 Typical application



4 Features

- Dynamic proximity switch with 8 sensor channels
- Support for matrix arrangement of sensors
- Direct and latching switch modes
- Digital processing method
- Continuous auto-calibration
- Sensing plates can be connected remotely
- I^2C Fast-mode Plus (Fm+) compatible interface
- Interrupt output
- Clock and interrupt cascading for two IC's possible
- Address LSB can be configured via external pin (two IC's can be addressed)
- Low-power battery operation possible (IDD ~ 10µA)
- Sleep mode (< 100nA)
- Adjustable response time
- Adjustable sensitivity
- Large voltage operating range (VDD = 2.5 to 5.5V)
- Temperature operating range Tamb = -40°C to 85°C
- Internal voltage regulator
- Available in 5x5mm QFN28 (other packages available for larger quantities)

5 Ordering Information

Table 1: Ordering information

Type	Package	Shipping	Article No.
MS8885B	QFN28 5x5mm	Tape&Reel	9160151

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6 Pinout

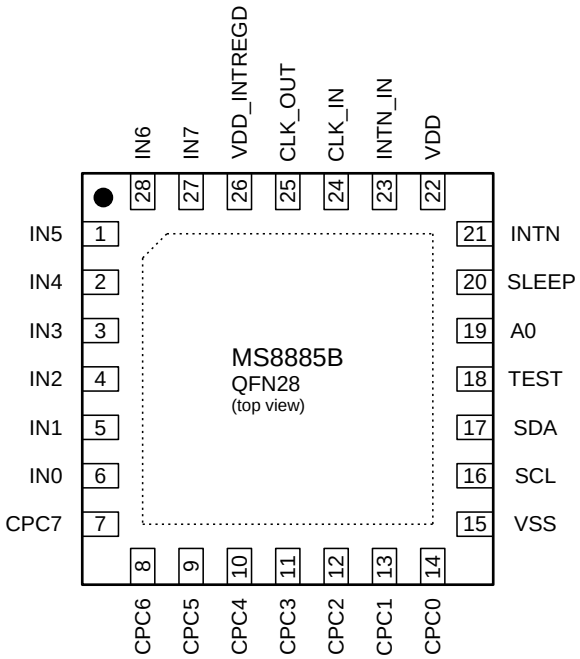

Figure 1: Pinout QFN28 (5x5mm)

7 Block diagram

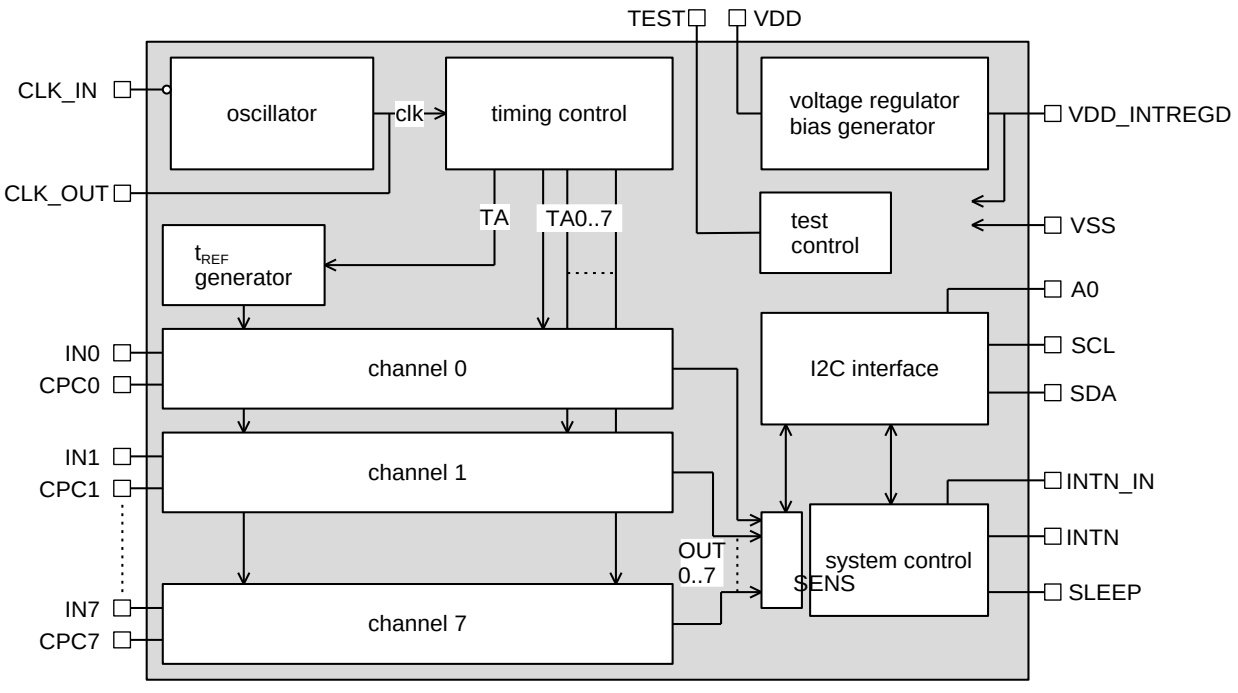

Figure 2: Block diagram

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8 Pin description

Table 2: Pin description

Pin TSSOP28	Pin QFN28	Symbol	I/O[1]	Description
26	22	VDD	S	positive supply
2	26	VDD_INTREGD	S	internal analog supply
19	15	VSS	S	negative supply
10…3	6...1 28,27	IN0 to IN7	A	sensor-Inputs, channels 0..7
18…11	14...7	CPC0 to CPC7	A	reservoir capacitor, channels 0..7
20	16	SCL	I/O	I^2C clock signal
21	17	SDA	I/O	I^2C data signal
23	19	A0	I	I^2C address LSB, used to address two devices, low -> address 0x3A, high -> address 0x3B (examples only)
25	21	INTN	O	interrupt output, low level when interrupt is activated
27	23	INTN_IN	I	interrupt input for device cascading, connect to VDD if not used
28	24	CLK_IN	I	clock input for 'secondary' device, when a clock is provided by the 'primary' device
1	25	CLK_OUT	O	clock output for device cascading/synchronization
22	18	TEST	A	test pin, should be connected to VSS in application
24	20	SLEEP	I	sleep mode, set to '1' to force the circuit into low-power sleep mode

9 Description

9.1 Basic functionality

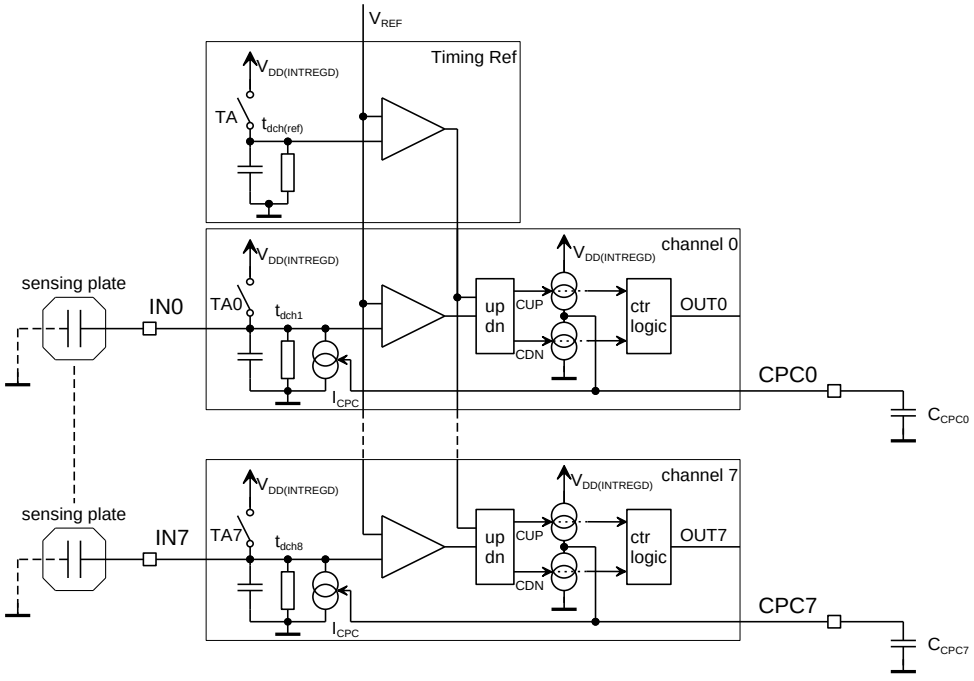

Figure 3: Functional diagram of sensor operation

Figure 3 illustrates the functional principle of the MS8885B. The discharge times t_{dchx} on inputs INx, attached to the sensing plate capacitances, are compared to the discharge time $t_{dch(ref)}$ of an internal RC timing element, for each sensor input sequentially. The RC timing circuits are periodically charged to $V_{DD(INTREGD)}$ via MOS switches and then discharged via a resistor to V_{SS}. The charge-discharge cycle for each channel is governed by the sampling

[1] I: Input, O: Output, S: Supply, A: Analogue

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rate (f_S). The channels are sampled sequentially, while the reference element is activated at the sampling point of each channel (see timing diagram in Figure 4). When the voltage of an RC combination falls below the V_{ref} level, the appropriate comparator output will change. The logic following the comparators determines which comparator switched first. If the reference comparator switches first, then a pulse is given on CUP. If the sensor comparator switches first then a pulse is given on CDN.

The pulses control the charge on the external capacitors CCPC on pins CPC0 to CPC7. Every time a pulse is given on CUP, capacitor CCPC is charged through a current source I_{src} from VDD(INTREGD) for a fixed time causing the voltage on CCPC to rise by a small increment. Likewise when a pulse occurs on CDN, capacitor CCPC is discharged through a current sink IDN towards ground for a fixed time, causing the voltage on CCPC to fall by a small decrement. The voltage on CCPC controls an additional current sink I_{sink} that causes the capacitance attached to the input pin I_{Nx} to be discharged more quickly. This arrangement constitutes a closed loop control system, that constantly tries to equalise the discharge time t_{dch} with $t_{dch(ref)}$. In the equilibrium state, the discharge times are nearly equal and the pulses alternate between CUP and CDN.

The counter following this logic counts the pulses CUP or CDN respectively. The counter is reset every time the pulse sequence changes from CUP to CDN or vice versa. The output OUT0 to OUT7 will only be activated when a sufficient number of consecutive CUP or CDN pulses occur. Low level interference or slow changes in the input capacitance do not cause the output to switch.

Various measures, such as asymmetrical charge and discharge steps, are taken to ensure that the output switches off correctly. A special start-up circuit ensures that the device reaches equilibrium quickly when the supply is attached.

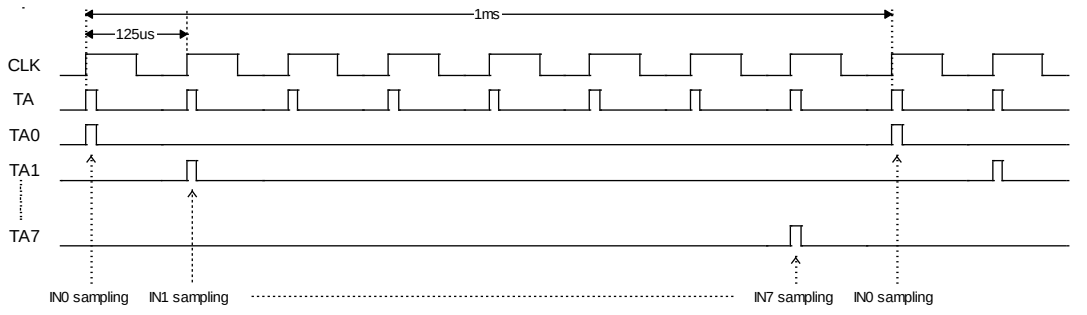

Figure 4: Timing diagram of sensor sampling

The sampling rate (f_s) is derived from the internally generated oscillator frequency. The oscillator frequency can be adjusted within a specified range by programming the CLKREG register.

The status of the signals OUT0 to OUT7 is stored in the SENS register (see Table 7). An interrupt is generated on changes of the sensor states.

9.2 Operating modes

The operating characteristics of the MS8885B can be configured by programming the CONFIG register:

- Main operating mode: stand-alone, primary, or secondary
- Switching mode: direct or latching
- Key-press mode: N-key, 2-key or 1-key
- Sleep mode

9.2.1 Main operating modes

The MS8885B can operate in three operating modes: ‘stand-alone’, ‘primary’ and ‘secondary’. The operating modes are implemented to support the application of two cascaded devices in the system, which is described in more detail in section 9.4 below. The modes are selected with the OPM bits in the configuration CONFIG register. The following table shows the main differences between the three modes.

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Table 3: Main operating modes

Mode	Clock source	Oscillator	Clock output	Comment
stand-alone	internal oscillator	enabled	disabled	default operating mode after power-on
primary	internal oscillator	enabled	enabled	
secondary	clock input	disabled	disabled	

The default operating mode after power-up is ‘stand-alone’.

9.2.2 Switching mode

Two switching modes are supported: direct and latching. The default switching mode after reset is direct mode. In **direct mode** the sensor state is directly reflected in the SENS register. When the sensor is activated, the corresponding bit in SENS is immediately set. When the sensor is released, the bit is cleared again. The bits are even cleared if the SENS register has not yet been read by the system controller. In **latching mode** every sensor-activation sets the corresponding bit in the SENS register. When the sensor is released, the SENS register is unaffected. Reading the SENS register resets those bits, whose sensor is not activated anymore.

9.2.3 Key press mode

There are three key-press modes implemented in the MS8885B.

In **N-key** mode each sensor activity is reflected in SENS, in accordance with the configured switching mode.

In **1-key** mode only the first sensor activation results in the corresponding bit being set in SENS. All further activations of the other sensors are suppressed at the SENS register boundary. In this way sensors in a keypad, which are activated accidentally because they are arranged next to the intended sensor, are masked out. The 1-key mode supports sensor matrix arrangements, where the columns and rows are attached to two separate (primary & secondary) MS8885B ICs. Only one row and one column sensor bit will be set in the SENS registers of the two devices. Each sensor-activation will raise an interrupt. The controller IC must handle the situation where the INTN is activated before the second sensor in the matrix has been activated.

In **2-key** mode only the two first sensor activations result in the corresponding bits being set in SENS. All further activations of the other sensors are suppressed at the SENS register boundary. This mode supports in particular the matrix arrangement of sensors, as illustrated in the application drawing in Figure 14 on page 13. In this way sensors in a matrix, which are activated accidentally because they are arranged next to the intended sensors, are masked out. This mode properly handles a delay in sensor activation due to unequal sensor capacitance/area, non-centric sensor touching, etc., as long as the intended sensors react before sensors which are accidentally activated.

The default key press mode after reset is N-key mode.

9.2.4 Channel masking

The channel masking register MASK allows individual sensor channels to be enabled or disabled for particular applications or certain modes (for example only the on/off sensor should be active).

When bit MSKMODE in CONFIG is set to ‘0’, the disabled channels will continue to be sampled, but switching events will not be reflected in SENS and will not cause an interrupt. When bit MSKMODE in CONFIG is set to ‘1’, only channels which are enabled are actually sampled. Reducing the number of sampled channels also reduces the power consumption.

When a channel becomes newly enabled, the fast start-up method is used to quickly reach the functional state.

9.2.5 Sleep mode

Sleep mode is implemented to save power during periods, where no sensor activity is expected or supported.

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In sleep mode most of the circuit parts are put in power down mode, in particular all analog blocks consuming static and dynamic power. This includes the oscillator, thus no internal activity remains. Also the voltage regulator is powered down, to reduce its standalone power consumption.

The I^2C interface is powered from V_{DD}. Therefore the system still remains responsive to I^2C activity.

During sleep mode the register configuration is maintained. The charges in the CPC capacitors however cannot be guaranteed, as there is no limitation on the duration of the sleep mode. Therefore the analog part has to perform a normal start-up phase, including the fast start procedure for the CPC capacitor charging.

Sleep mode is entered when the SLEEP command is received from the system controller or when the SLEEP pin is set to high.

Wake-up from sleep is through the WAKE command, or by setting the SLEEP pin to low.

9.3 Interrupt generation

The MS8885B provides two mechanisms to inform the system controller, that a sensor activity has been detected.

9.3.1 Interrupt output INTN

The MS8885B has an interrupt output INTN, to flag to the system controller that a capacitive event has been detected. The controller can then fetch the sensor state by reading the SENS register over the I^2C bus. The interrupt generation is controlled by the INTM bit of the CONFIG register:

- If INTM is '0' (default) then each bit change in SENS (set or clear) activates the INTN output.
- If INTM is '1', then only sensor press events, resulting in bits being set in SENS, activate the INTN output. Sensor release events which cause the corresponding bit in SENS to be cleared don't activate the INTN output.

In 2-key mode the INTN output is only activated after two bits have been set in the SENS register. The interrupt is automatically cleared when the system controller reads the SENS register. Alternatively the interrupt can be cleared using the CLINT command, without reading the actual sensor state.

The INTN pin is low active. When no interrupt is active, the INTN pin is at VDD level. It is pulled to VSS level when an interrupt is signalled.

9.3.2 Interrupt over the I^2C bus

In order to flag an interrupt over the I^2C bus, the MS8885B behaves like an I^2C master with restricted functionality. The interrupt is signalled by sending a START condition, immediately followed by a STOP condition. This is illustrated in Figure 5. No further I^2C master capabilities are supported.

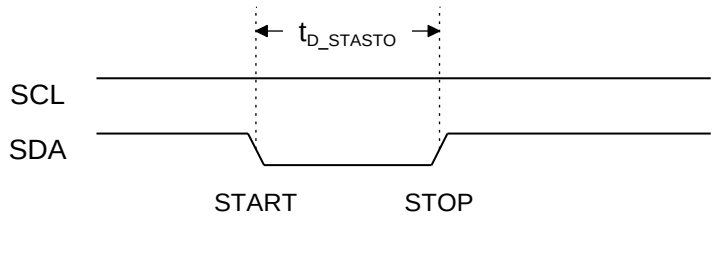

Figure 5: Interrupt over I^2C bus

The system controller has to detect the START-STOP condition and react accordingly.

In order to enable this mode, the MS8885B has to be put in int-over-I^2C mode. This is done with the INTI^{2}C command. In reset state the int-over-I^2C mode is disabled. In int-over-I^2C mode the INTN functionality continues to work in the normal way.

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9.4 Device cascading

Two MS8885B devices can be connected to the same I²C bus, which facilitates up to 8x8 keypads.

The device provides the following features to guarantee robust operation and to simplify the system design using two devices:

- The 7-bit I²C address consists of 6 fixed bits and 1 selectable bit. The level externally applied to pin A0 (V_{DD} or V_{SS}) defines the LSB of the I²C address. In this way two MS8885B can be addressed on the same bus without the need for different silicon versions with hard coded I²C addresses.
- The sensor activity can be synchronized, so that interference between the sensors of the different devices is avoided. One device is considered to be the 'primary' device. It provides the sample clock on pin CLK_OUT. The other device is considered to be the 'secondary' device. It uses the clock provided by the 'primary' device instead of the internal clock. The 'primary' device samples the sensors on the rising edge of the internal sample clock. The CLK_IN signal is inverted to derive the sample clock in the 'secondary' device. Therefore the 'secondary' device samples its sensors on the negative edge of the primary's sample clock. In this way no simultaneous sensor sampling occurs. 'Primary' or 'secondary' modes are enabled by programming the configuration register.
- The interrupt signal can be cascaded. The INTN output of the 'primary' device can be connected to the INTN_IN input of the 'secondary' device. The INTN output of the 'secondary' device is then an OR'ed combination of the two interrupts.
- If two devices are cascaded and the int-over-I²C mode is desired, then it is sufficient to put the 'secondary' device in int-over-I²C mode. The 'primary' device still signals an interrupt over the INTN output to the INTN_IN input of the 'secondary' device.

Figure 14 on page 13 illustrates a typical example of an application using two MS8885B circuits.

9.5 Clock generation

The MS8885B contains an integrated oscillator as main clock source. The oscillator runs nominally at f_{OSC}=128 kHz. The internal clock frequency f_{clk} is derived from the oscillator clock by division by 1, 4, 16 or 64.

The eight sensors are sampled sequentially, which results in a default sensor sampling rate of f_s = 1 kS/s.

In slave mode the internal clock generator is stopped, and the circuit is clocked from the CLK_IN input pin.

9.5.1 Frequency adjustment

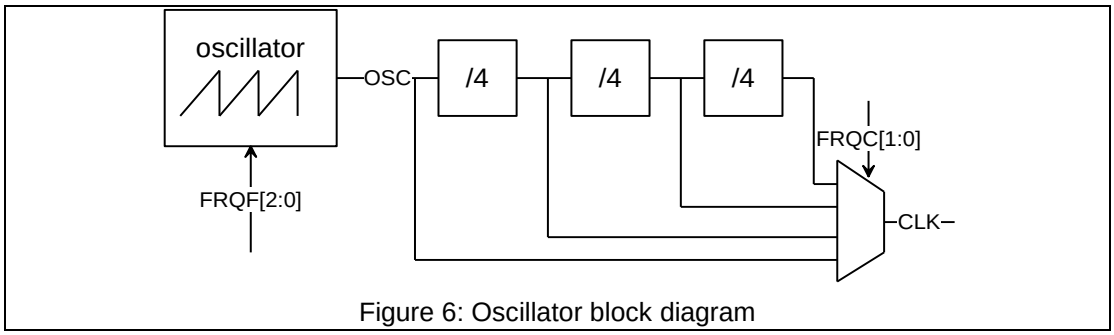

Figure 6: Oscillator block diagram

The frequency of the internal oscillator can be adjusted, and the programmable clock divider allows changing the sensor sampling rate further. This way the reaction time and power consumption of the circuit can be adjusted over a wide range.

The frequency settings are controlled by the CLKREG register with the bits FRQC[1:0] and FRQF[2:0] (details in section 10.3.4).

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9.6 Power architecture, reset concept, and start-up behaviour

9.6.1 Power Architecture

The circuit has an integrated voltage regulator, supplied from pin V_{DD}. The regulator provides an internal $V_{DD(INTREGD)}$ supply of nominally 2.8V.

If a stable and noise free external supply voltage with 2.5V < $V_{DD(ext)}$ < 3.0V is available in the system, $V_{DD(INTREGD)}$ can be provided from the external source. In this case V_{DD} and $V_{DD(INTREGD)}$ must both be connected to $V_{DD(ext)}$, and the internal regulator can be shut down in order to reduce the current consumption.

While the analog part of the circuit is powered from $V_{DD(INTREGD)}$, the I^2C interface and the registers are powered from V_{DD}. Therefore the I^2C interface remains accessible in sleep mode, and the register values are maintained when $V_{DD(INTREGD)}$ is powered off.

9.6.2 Reset mechanism

Reset takes place during power-up of the circuit. There is no external hardware reset input.

During operation the device can be reset using the SRES command. The SRES resets all registers to their default values. It does not affect the state of the analog section except for those functions that are controlled by configuration bits.

9.6.3 Start-up procedure

After power-up of V_{DD} the registers in the V_{DD} domain are reset, which includes the VROF bit controlling the voltage regulator. The regulator is therefore enabled, and the $V_{DD(INTREGD)}$ domain is powered up. As soon as a sufficient $V_{DD(INTREGD)}$ level is reached, the POR is released.

After release of the POR in the $V_{DD(INTREGD)}$ domain, the circuit starts with the sensor sampling in the fast start mode (increased charge-pump currents quickly charge the CPC capacitors close to their target value). As soon as the capacitor voltages are close to the target value, the fast start phase is terminated, and the capacitors are charged in fine steps to the final value. When this state is reached, the logic enables the up/down counters, and the sensors are operational.

This start-up mechanism is executed independently in each channel.

10 I^2C serial interface

The MS8885B has an I^2C serial interface which operates as a slave receiver or transmitter. SDA and SCL are the data I/O and clock lines for the serial I^2C Interface. SDA is used as an input or as an open-drain output. SDA is actively pulled low and is passively held high by the external pull-up resistor on the I^2C bus.

In order to provide high link robustness, the I^2C interface of the MS8885B is Fast-mode Plus (Fm+) compatible.

10.1 Supported I^2C protocol

The following symbol set is used in the subsequent figures showing the I^2C protocol:

- S = START symbol
- P = STOP symbol
- A = ACKNOWLEDGE bit
- = sent from MS8885B
- = sent from I^2C Master

10.1.1 Addressing

Figure 7 below shows the most basic transmission. It is useful to explain the addressing scheme.

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The 7-bit I²C address is composed of the 6 fixed base address bits ‘aaaaaa’ and the sub-address bit ‘sa’. The I²C slave is addressed correctly, if the base address ‘aaaaaa’ matches the hard programmed address, and if the ‘sa’ bit matches the logic level on pin A0.

Therefore two identical MS8885B devices can be addressed, if one of them has A0 tied to logic ‘0’, and the other one has A0 tied to logic ‘1’.

The base address reserved for the MS8885B is ‘aaaaaa’ = ‘010000’.

	I²C slave address							
Bit	7	6	5	4	3	2	1	0
	0	1	0	0	0	0	A0	R/W

10.1.2 I²C Master writes command without data

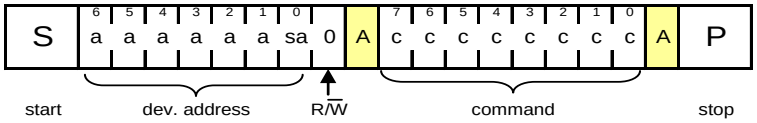

Figure 7: I²C command transmission

This protocol is used, if the I²C master only needs to send a single command to the MS8885B without additional data. The 8-bit command ‘cccccccc’ is transmitted in the 1st data byte.

10.1.3 I²C Master writes one data byte

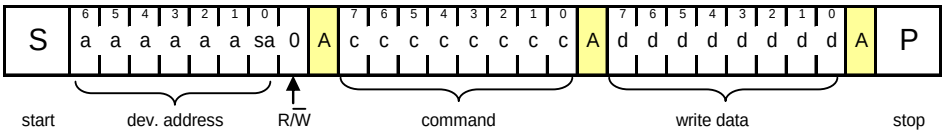

Figure 8: I²C write data transmission

This protocol is used, when the I²C master needs to program a register. The command part ‘cccccccc’ then specifies the write register command, including the selection of the register. The data byte contains the register content to be written.

10.1.4 I²C Master reads one data byte

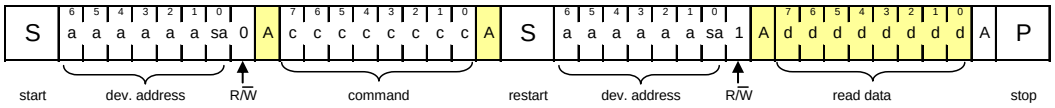

Figure 9: I²C read data transmission

In order to read a register, the I²C master first has to send the corresponding read command. Therefore the transmission starts with a command-write sequence. After this the transmission is not stopped, rather a restart (second START symbol) is sent, followed by a retransmission of the address. In this second start the R/W bit is set to ‘1’, indicating to the slave that it must transmit the data byte.

10.1.5 I²C Master reads sensor data

The MS8885B supports direct reading of the sensor state from SENS register. If - after sending the address - the R/W bit is immediately set to ‘1’ without sending a command, the circuit recognises that it must immediately return the content of the SENS register.

This transaction is illustrated in Figure 10.

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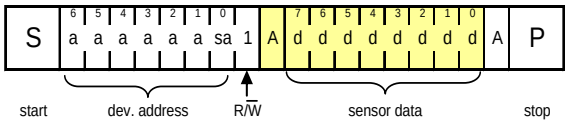

Figure 10: I²C read sensor data

When the transaction after reading the SENS register is not terminated with the STOP symbol, the MS8885B repeatedly sends the content of SENS again. This provides a means to continuously observe the sensor activity. This transaction is illustrated in Figure 11.

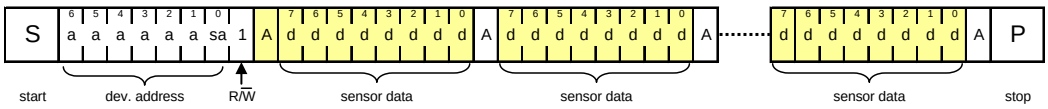

Figure 11: I²C read sensor data continuously

If two MS8885B are used in a cascaded configuration (Section 9.4) one is in the 'primary' and the other is in the 'secondary' role. When the direct read transaction is executed in a cascaded configuration, the 'primary' device transmits its SENS content register immediately after the address byte, followed by the 'secondary' device transmitting its SENS register content.

If the transaction after reading the two SENS registers is not terminated with the STOP symbol, the 'primary' and 'secondary' MS8885B continue sending the content of the SENS registers alternately. Such a transaction is illustrated in Figure 12.

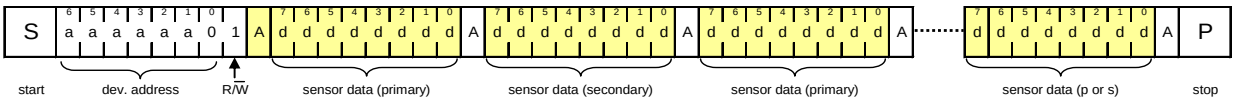

Figure 12: I²C read sensor data, alternately from master & slave

It must be noted, that for this alternate data transfer only one MS8885B has to be addressed. By definition the 'primary' device must be addressed (sa bit set in the address set to '0'). In this particular case the 'secondary' device reacts on the address of the 'primary' device. For all other transactions targeting the 'secondary' device, it must be properly addressed with sa set to '1'.

10.2 I²C command descriptions

Table 4: Supported I²C bus commands

OpCode	Symbol	Command name	Function	Transfer type
'0000 0000'	SRES	soft-reset	soft reset, brings device to reset state	command
'0000 0011'	CLINT	clear-INTN	clear INTN line	command
'0000 0101'	SLEEP	sleep	enter sleep state	command
'0000 0110'	WAKE	wake	enter active state	command
'0011 0000'	CFGWR	write-config	write configuration register	write 1 Byte
'0011 0011'	CFGRD	read-config	read configuration register	read 1 Byte
'0011 0101'	CLKWR	write-clock	write clock setting register	write 1 Byte
'0011 0110'	CLKRD	read-clock	read clock setting register	read 1 Byte
'0011 1001'	MSKWR	write-mask	write the mask register	write 1 Byte
'0011 1010'	MSKRD	read-mask	read the mask register	write 1 Byte
'0011 1100'	INTI2C	int-over-I²C	put the device in int-over-I²C mode	command
direct read	SENSRD	read-sensor	read sensor state register (clears INTN)	read N bytes

Several configuration settings can be programmed using single commands without associated data transfer. The configuration register can however also be written using the write data command (CFGWR). The clock and mask registers can only be programmed using the write data commands (CLKWR, MSKWR).

10.2.1 SRES command

Performs a soft reset of the circuit. Resets all registers to default values. Resets sensor channels. Exits int-over-I²C mode. See Section 9.6.2 on page 8.

10.2.2 CLINT command

This command deactivates the interrupt line, without reading the sensor state register SRES.

10.2.3 CFGWR / CFGRD commands

These commands are used to write and read the complete configuration register.

10.2.4 CLKWR / CLKRD command

Used to write and read the complete clock setting register, mainly allowing the internal oscillator frequency to be tuned.

10.2.5 MSKWR / MASKRD commands

Used to write and read the MASK register.

10.2.6 INTI2C command

The MS8885B is put into int-over-I^2C mode to enable an interrupt signalling over the I^2C lines. This mode is described in more detail in Section 9.3.2 on page 6.

10.2.7 SENSRD command

This is the main transaction to read the actual sensor state information.

If the R/W bit is set to '1' immediately after the address bits, the MS8885B interprets the transaction as the SENSRD command.

The SENSRD transaction supports a repeated reading of the SENS register.

When two circuits are used in a cascaded configuration, the two circuits alternately return their SENS register content in a single transaction.

The protocols for the repeated read mode and alternating read mode are described in Section 10.1.5 in detail.

10.3 Register descriptions

10.3.1 Register overview

Table 5 Register overview

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset value
CONFIG	OPM[1:0]		SWM	KM[1:0]		VROF	INTM	MSKMODE	'0000 0000'
SENS	CH[7:0]								'0000 0000'
CLKREG	CLO	CLI	n/a	FRQC[1:0]		FRQF[2:0]			'00-0 1100'
MASK	MSK[7:0]								'1111 1111'

10.3.2 CONFIG: Configuration register

Table 6 CONFIG - configuration register, bit description

Bit(s)	Symbol	Function	Reset value
7:6	OPM[1:0]	main operating mode '00': stand-alone mode '01': 'secondary' mode '10': 'primary' mode '11': n/a	'00'
5	SWM	switching mode '0': direct switching mode (sensor release clears bit in SENS) '1': latching mode (reading SENS clears bit in SENS)	'0'
4:3	KM[1:0]	key press mode '00': N-key mode, each sensor activity is reflected in SENS '01': 2-key mode, only first two keys are visible in SENS '10': 1-key mode, only first key press is visible in SENS	'00'
2	VROF	voltage regulator off	'0'
1	INTM	interrupt generation mode '0': Interrupt is generated on each SENS bit change, press and release	'0'

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		'1': Interrupt is generated on bits being set in SENS (press only)	
0	MSKMODE	channel masking mode '0': normal power: masked out channels remain operational '1': low power: masked out channels are powered down	'0'

All bits in this register can be written and read.

10.3.3 SENS: Sensor state register

Table 7 SENS - sensor state register, bit description

Bit(s)	Symbol	Function	Reset value
7:0	CH[7:0]	sensor state of respective channels IN7 to IN0	'0000 0000'

All bits in this register are read-only.

10.3.4 CLKREG: Clock setting register

Table 8 CLKREG - clock setting register, bit description

Bit(s)	Symbol	Function	Reset value
7	CLO	CLK_OUT enable '0': CLK_OUT is disabled (unless device is in 'primary' mode) '1': CLK_OUT is enabled	'0'
6	CLI	CLK_IN enable '0': CLK_IN is disabled, (unless device is in 'secondary' mode) '1': CLK_IN is enabled, and internal oscillator is powered down	'0'
5	n/a	n/a	n/a
4:3	FRQC[1:0]	sampling clock frequency, coarse setting '00', nominal sampling rate: $f_{clk} = f_{osc} / 64$ '01', nominal sampling rate: $f_{clk} = f_{osc} / 16$ '10', nominal sampling rate: $f_{clk} = f_{osc} / 4$ '11', nominal sampling rate: $f_{clk} = f_{osc}$	'01'
2:0	FRQF[2:0]	oscillator tuning '000' min. frequency: $f_{osc} \approx 0.5 \cdot f_{osc,nom}$ … '100' typical frequency: $f_{osc} \approx f_{osc,nom}$ … '111' max. frequency: $f_{osc} \approx 2 \cdot f_{osc,nom}$	'100'

All bits in this register can be written and read. Bit 5 should be written with logic 0 and if read, it can be either logic 0 or logic 1.

10.3.5 MASK: Channel enable mask register

Table 9 MASK - channel enable mask register, bit description

Bit(s)	Symbol	Function	Reset value
7:0	MSK[7:0]	enable / disable individual sensor channels IN7 to IN0 '0': sensor channel is disabled '1': sensor channel is enabled	'1111 1111'

All bits in this register can be written and read.

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10.4 I²C interface timing

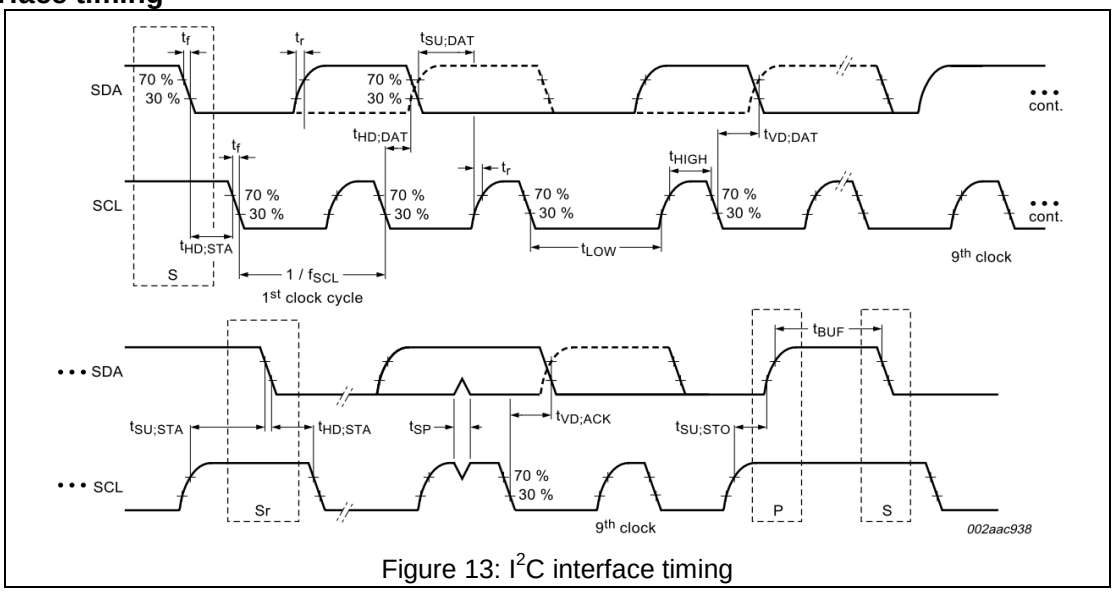

Figure 13: I²C interface timing

The timing figures are specified in Section12 0.

11 Application design-in information

Figure 14 below shows the typical connections for a general application using two devices. For simplicity, the sensors attached to the 'secondary' device are not shown in this diagram. The sensors of the 'secondary' device can be arranged independently of the sensors of the 'primary' one or combined in a common larger matrix.

Both devices use different I²C addresses programmed by the voltage level applied to pin A0. The 'primary' circuit has A0 connected to ground; the 'secondary' one has A0 connected to V_{EXT}. In this way each circuit is addressed individually.

The 'primary' device is configured to use the internal oscillator as clock reference. It is also programmed to enable the clock output. The 'secondary' device is programmed to use the clock output from the 'primary' device as input clock. The internal oscillator of the 'secondary' device is shut down to save power in this mode.

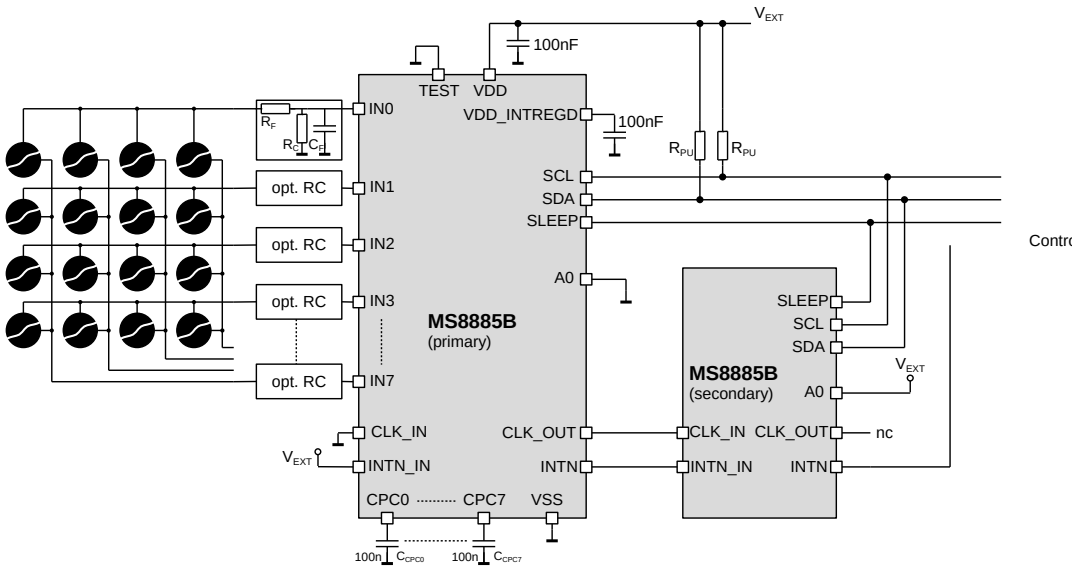

Figure 14: Typical application schematic

The interrupt output INTN of the 'primary' is routed to the INTN_IN input of the 'secondary' device, where it will be OR'ed with the interrupt state of the 'secondary'.

The sensing plate capacitances may consist of a small metal area, for example behind an isolating layer. Illustrated in Figure 14 is a 4x4 sensor arrangement. In this configuration, a sensor touch always excites two sensor plates at the same time.

The sensing plates are connected to a coaxial cable (for remote sensors) or a shielded connection, which in turn is connected to the input pin IN. The connection capacitance contributes to the input capacitance and must not be neglected. An internal low pass filter (not shown) is used to reduce RF interference. An additional low pass filter consisting of a resistor R_F and capacitor C_F can be added to the input to further improve RF immunity as required. For good performance, the total amount of capacitance on the input (C_S+C_{CABLE}+C_F) should be in the proper range, the optimum point being around 30pF. Even if the external filtering is not required, placing C_F can help to bring the input capacitance to an optimal value. These conditions allow the control loop to adapt to the static capacitance on C_S of the sensor and to compensate for slow changes in the sensing plate capacitance. A higher capacitive input loading is possible provided that an additional discharge resistor R_C is used. Resistor R_C simply reduces the discharge time such that the internal timing requirements can be fulfilled.

The sensitivity of the sensors can be influenced by the sensing plate area and capacitors C_{CPC}. The sensitivity is significantly reduced when C_{CPC} is reduced. When maximum sensitivity is desired C_{CPC} can be increased, but this also increases sensitivity to interference. The CPC0 to CPC7 pins have high impedance and are sensitive to leakage currents. Therefore C_{CPC} should be a high quality foil or ceramic capacitor, for example an X7R type.

For the choice of proper component values for a given application, the component specifications in Section 12.2 must be followed.

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12 Electrical Characteristics

12.1 Limiting values

Name	Parameter		Min	Max	Unit
V_{DD}	positive supply		-0.5	8.0	V
$V_{DD(INTREGD)}$	internal regulated supply		-0.5	6.5	V
V_I	input voltage, on all input pins		-0.5	6.5	V
I_{SS}	total current to V_{SS}		-50	50	mA
I_n	current through any pin, except SDA		-10	10	mA
I_{SDA}	current through SDA pin		-30	30	mA
P_{tot}	power dissipation			100	mW
V_{ESD}	electrostatic discharge voltage	HBM CDM		± 2000 ± 500	V V
I_{lu}	latch-up current, at 85°C			+/- 100	mA
T_{stg}	storage temperature		-60	+125	°C

Notes:

- Values exceeding the limiting values may cause permanent damage to the device.
- Inputs and outputs of the MS8885B are protected against electrostatic discharges (ESD) during normal handling. However to be totally safe, it is advisable to undertake handling precautions appropriate to handling MOS devices.

12.2 Static Characteristics

Conditions: V_{DD} = 3.0V DC, V_{SS}=0V, T_{amb} = 25°C, if not stated otherwise

Symbol	Parameter	Conditions / Comment	Min	Typ	Max	Unit
V_{DD}	positive supply		2.5		5.5	V
$V_{DD(ext)}$	external supply	V_{DD} connected to $V_{DD(INTREGD)}$ and internal regulator disabled	2.5		3.3	V
$V_{DD(INTREGD)}$	regulated internal supply	$V_{DD} > V_{lockin}$	2.5	2.9	3.3	V
$\Delta V_{DD(INTREGD)}$	regulator voltage drop	$V_{DD} < V_{lockin}$, no external load on $V_{DD(INTREGD)}$		10		mV
I_{DD}	operating current	idle state[1], output inactive, f_s = 1 kHz		10	20	µA
$I_{DD(sleep)}$	sleep mode supply current	sleep mode		100	500	nA
Digital inputs (CLK_IN, A0, INTN_IN, SLEEP)						
V_{IL}	input LOW voltage		V_{SS}		$0.3V_{DD}$	V
V_{IH}	input HIGH voltage		$0.7V_{DD}$		V_{DD}	V
Digital outputs (INTN, CLK_OUT)						
V_{OL}	output LOW voltage	I_{OUT} = 0.5mA	V_{SS}		$0.2V_{DD}$	V
V_{OH}	output HIGH voltage	I_{OUT} = 0.5mA	$0.8V_{DD}$		V_{DD}	V
Analog pins (IN0 to IN7, CPC0 to CPC7)						
V_{CPC}	reservoir capacitor voltage on pins CPCx	usable control range	V_{SS}		$V_{DD(INTREGD)}$ – 0.3	V
C_i	input capacitance range (sensing plate & parasitic)		10		50	pF
I^2C interface pins (SDA, SCL, see I^2C Fm+ specification [1])						
V_{IL}	input LOW voltage		-0.5		$0.3V_{DD}$	V
V_{IH}	input HIGH voltage		$0.7V_{DD}$		5.5	V
I_{OL}	output LOW current	V_{OL} = 0.4V, SDA only	20			mA
I_L	leakage current		-1		+1	µA
C_i	pin capacitance				10	pF
External components						
C_{CPC}	reservoir capacitor	low leakage X7R ceramic type recommended	22	100	470	nF
$I_{L(CPC)}$	reservoir capacitor	low leakage X7R ceramic	-1		1	nA

[1] Idle state is the steady state after completed power-up, without any mode change and without any activity on the sensor plate and the voltages on the reservoir capacitors C_{CPC} are settled.

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	leakage current	type recommended				
C_{dec}	decoupling capacitance	on pin V_{DD} and $V_{DD(INTREGD)}$, ceramic chip capacitor		100		nF
Temperature range						
T_{amb}	operating temperature range		-40	25	85	°C

12.3 Dynamic Characteristics

Conditions: V_{DD} = 3.0V DC, V_{SS}=0V, T_{amb} = 25°C, if not stated otherwise

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
System timing						
$t_{startup}$	power-on start-up time	CCPC = 100nF, fs = 1 kHz[1]		400		ms
f_{osc}	internal RC oscillator frequency	FRQF[2:0]='111'		125		kHz
		FRQF[2:0]='100' (default)		80		kHz
		FRQF[2:0]='000'		40		kHz
t_{SW}	reaction time on sensor capacitance change	f_s = 1 kHz		64		ms
I^2C interface characteristics (SDA, SCL, see [1])						
t_{SP}	pulse width of spikes that must be suppressed by the input filter		0		50	ns
f_{SCL}	SCL clock frequency		0		1000	kHz
$t_{HD,STA}$	hold time START cond.		0.26			µs
$t_{SU,STA}$	setup time START cond.		0.26			µs
t_{LOW}	LOW period of SCL		0.5			µs
t_{HIGH}	HIGH period of SCL		0.26			µs
$t_{HD,DAT}$	data hold time		0			µs
$t_{SU,DAT}$	data setup time		50			ns
t_r	rise time SDA, SCL				120	ns
t_f	fall time SDA, SCL				120	ns
$t_{SU,STO}$	setup time STOP cond.		0.26			µs
t_{BUF}	bus free time between a START and STOP cond.		0.5			µs
C_b	capacitive load for each bus line				550	pF
$t_{VD,DAT}$	data valid time				0.45	µs
$t_{VD,ACK}$	acknowledge valid time				0.45	µs
t_{D_STASTO}	Duration of int-over-I^2C pulse on SDA line			2		µs

[1] The sampling frequency fs is described in section 9.5 on page 7.

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13 Package outline drawings

Package dimensions QFN28 (JEDEC MO-220-VHHD-3)

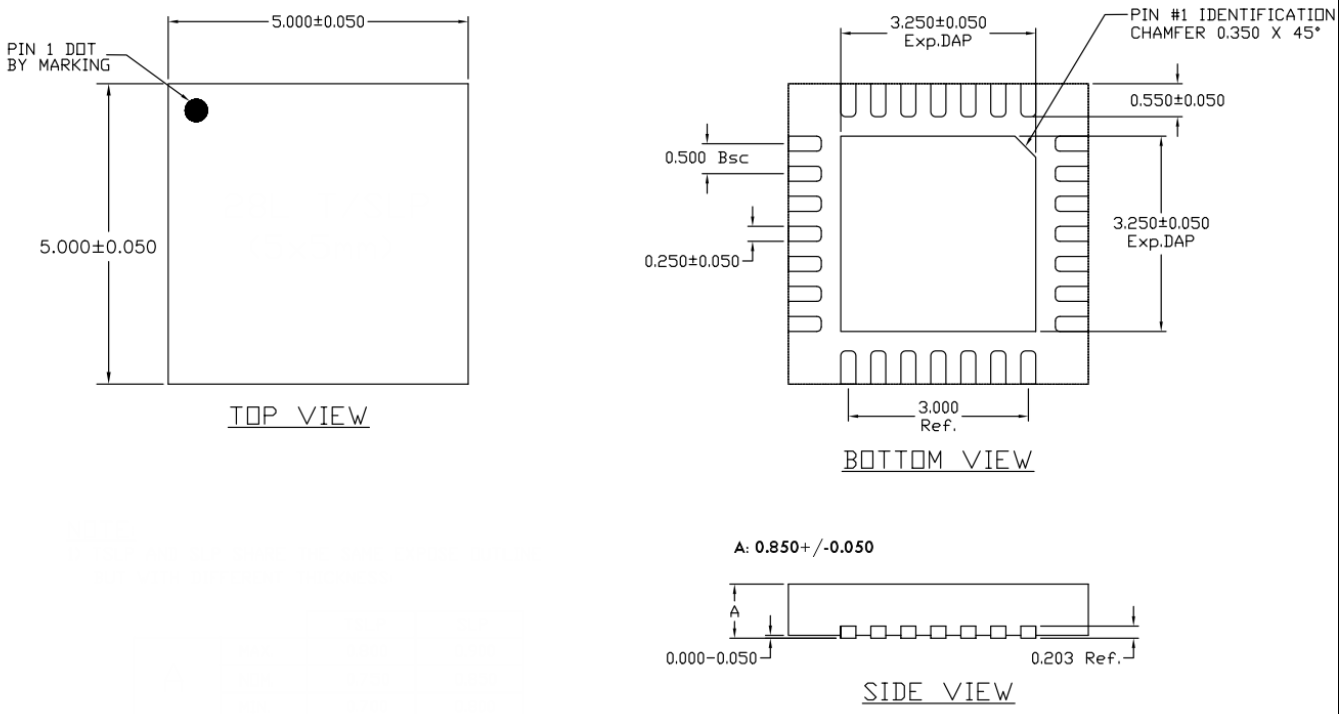

Figure 15: Package outline of MS8885B (QFN28)

14 Terms and abbreviations

Name	Definition
Fast-start mode	After power-up or soft-reset the sensor channels are put in a fast starting mode, where the charge pump currents are strongly increased to reach the idle state quickly. During the fast-start mode the circuit is not ready for touch sensing.
Idle state	State where the circuit is settled, tracks adaptively slow environment changes, and is ready to detect touching events. Each channel has its own idle state.
Fast-mode Plus (Fm+)	The I^2C specification distinguishes three modes with different electrical characteristics [1]. Fm+ is one of these modes.
I^2C master & slave	The I^2C master device controls the I^2C bus and initiates transactions. The MS8885B is always an I^2C slave device.
MS8885B primary & secondary device	In a two-chip application the two circuits can be cascaded and synchronized. In this case one device is considered the primary device (providing clock), and the other device is considered the secondary one.

15 Legal disclaimer

This product is not designed for use in life support appliances or systems where malfunction of these parts can reasonably be expected to result in personal injury. Customers using or selling this product for use in such appliances do so at their own risk and agree to fully indemnify Microdul AG for any damages resulting from such applications.

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